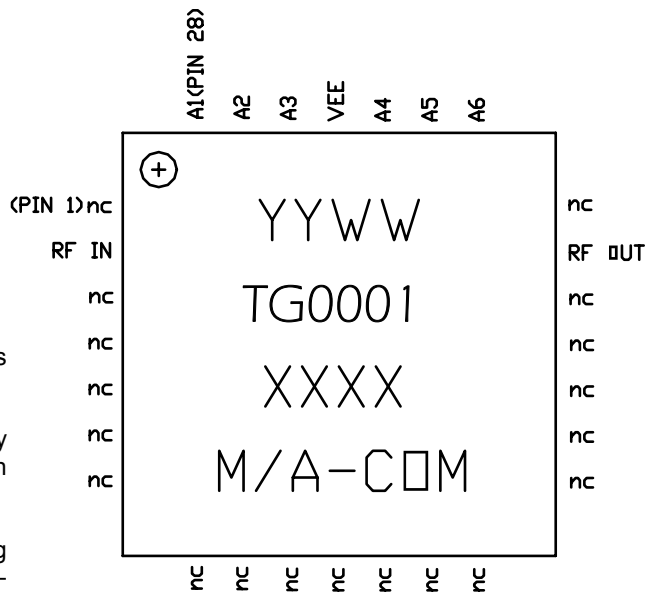
Attenuator
dc – 6.0 GHz

Features

- 6 Bit Attenuator Range
- 35dB Coverage, LSB = 0.56dB
- TTL Control Inputs
- MSAG™ Process
- 5mm, 28 Lead, PQFN Package



Description

The MAATGM0001 is a 6-bit Attenuator with Parallel Input Control. This product is fully matched to 50 ohms on both the input and output.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- Satellite Communication
- Phased Array Radar

Maximum Ratings[1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	36	dBm
Source Supply Voltage	V_{EE}	-6	V
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[2]

Characteristic	Symbol	Min	Typ	Max	Unit
Control Voltage	A1 thru A6				
Logic High		2.8	5	5	V
Logic Low		0	0	0.8	V
Junction Temperature	T_J			150	°C
Digital Supply Voltage	V_{EE}	-5.2	-5	-4.8	V

2. Operation outside of these ranges may reduce product reliability.

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Electrical Characteristics: T_B = 25°C, Z_0 = 50Ω, V_{EE} = -5V

Parameter	Symbol	Typical	Units
Bandwidth	f	dc - 6	GHz
Reference State Insertion Loss	IL	4	dB
Input VSWR (All States)	VSWR	1.5:1	
Output VSWR (All States)	VSWR	1.5:1	
RMS Attenuation Error	RMS	2	dB
RMS Attenuation Error — Calibrated	RMS	0.2	dB
Attenuation Range	ΔG	35	dB
Phase Variation over all Attenuator settings	ΔΦ	<8	°
Digital Supply Current	IEE	<10	mA
Input Third Order Intercept	ITOI	36	dBm
Input 1-dB Compression Point	P_{1dB}	26	dBm

Truth Table[3]

Pin	Designation	Description	Level	State
22	A6	18.0dB Attenuation Bit : MSB	Logic High	Attenuation ≈ 18.0dB
23	A5	9.0dB Attenuation Bit	Logic High	Attenuation ≈ 9.0dB
24	A4	4.5dB Attenuation Bit	Logic High	Attenuation ≈ 4.5dB
25	V_{EE}	DC Suply Voltage	-5V	ON
26	A3	2.25db Attenuation Bit	Logic High	Attenuation ≈ 2.25dB
27	A2	1.12dB Attenuation Bit	Logic High	Attenuation ≈ 1.12dB
28	A1	0.56dB Attenuation Bit : LSB	Logic High	Attenuation ≈ 0.56dB

3. All Attenuation Bits at Logic Low = Reference State.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{EE} = -5 V.
2. Apply Logic Voltages to control circuit as listed in Recommended Operating Conditions Table.
3. Power Down. Set V_{EE} = 0.

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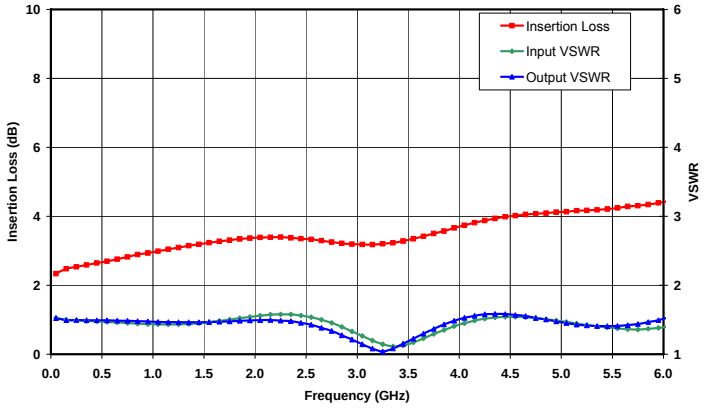

Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency

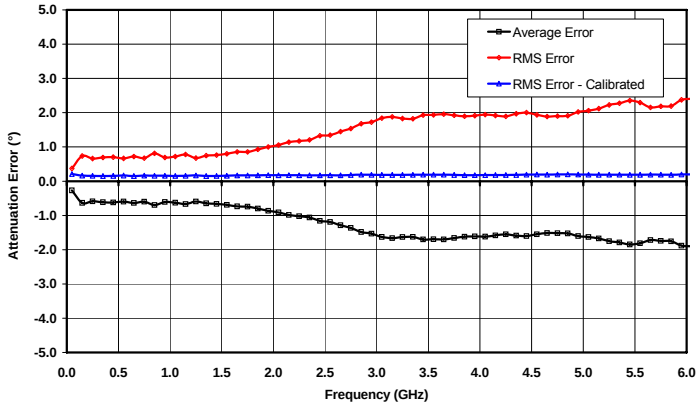

Figure 2. Attenuator Figures of Merit: Average Error,
RMS Error, and Calibrated RMS Error Over All States vs. Frequency

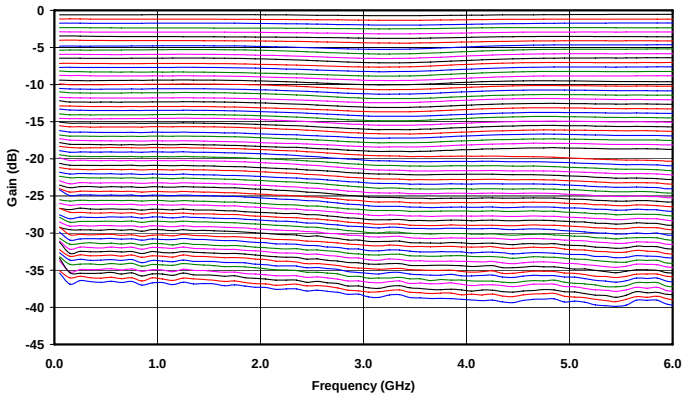

Figure 3. Relative Gain vs. Frequency Over All Attenuator States

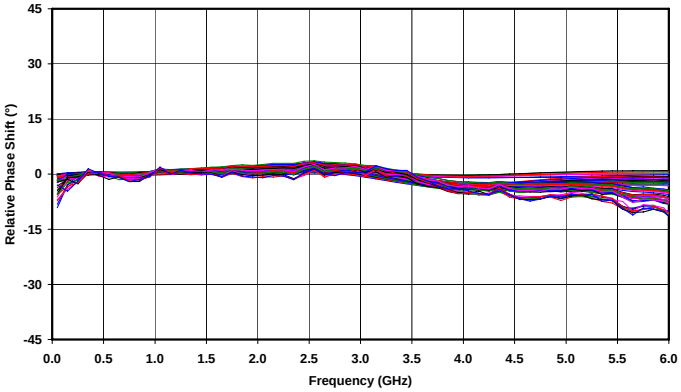

Figure 4. Relative Phase Shift vs. Frequency Over All Attenuator States

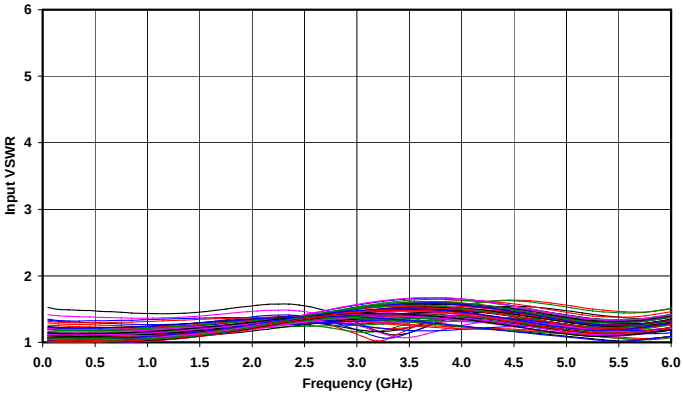

Figure 5. Input VSWR vs. Frequency Over All Attenuator States

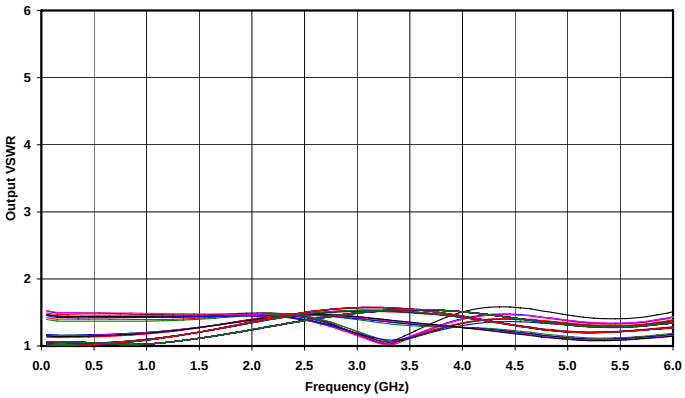

Figure 6. Output VSWR vs. Frequency Over All Attenuator States

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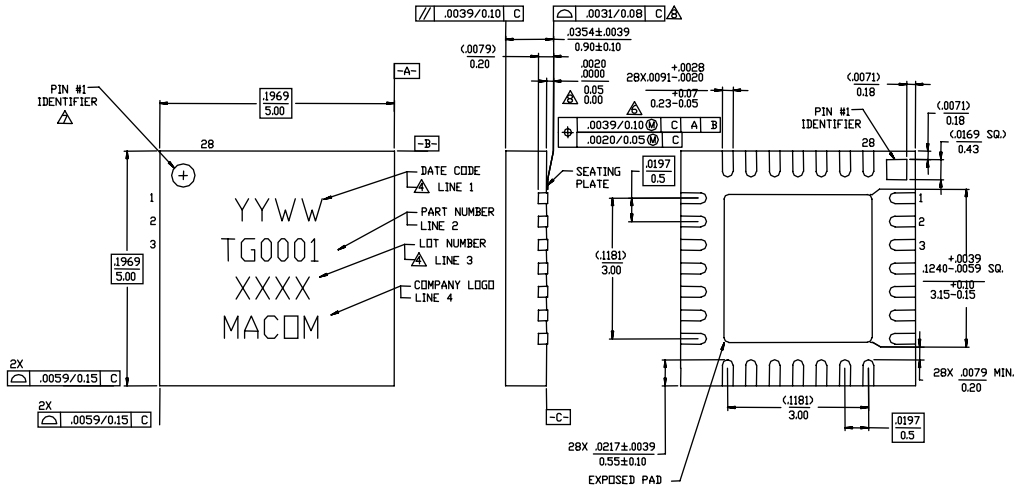

Figure 7. 5mm PQFN 28 Lead Package Drawing

Reference JEDEC M0-220 (see http://www.jedec.org), VAR. VJJC-3 (Issue E) for additional dimensional and tolerance information.

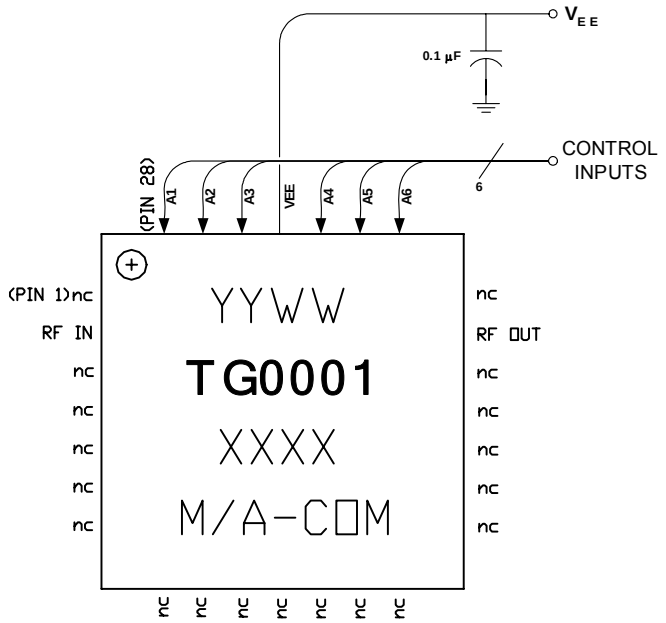

Figure 8. Recommended Bias Configuration

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note ***Surface Mounting Instructions for PQFN Packages #S2083**** for assembly guidelines.

Additional Precaution: All parts must receive a bake-out of 125ºC for 24 hours prior to any solder reflow operation.

*Application Notes can be found by going to the Site Search Page of M/A-COM's web page (http://www.macom.com/search/search.jsp) and searching for the required Application Note.

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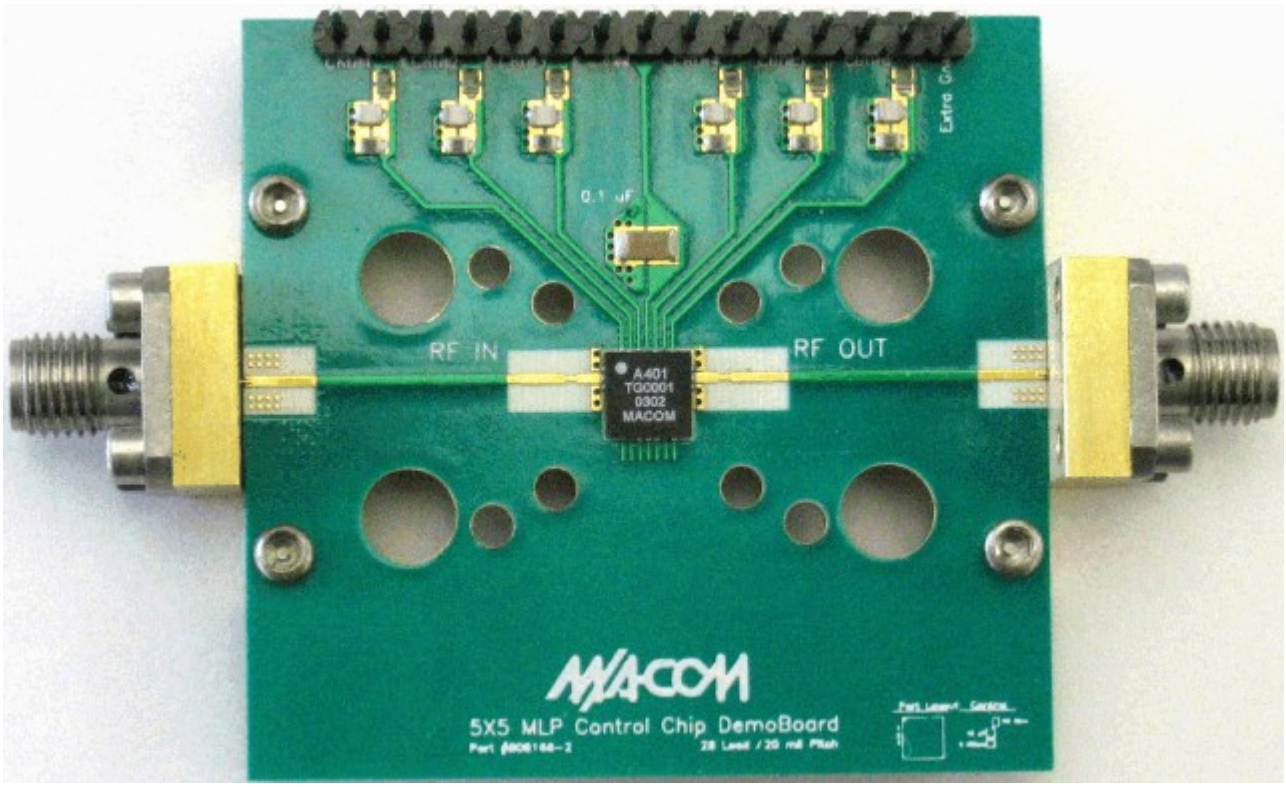

Figure 9. Demonstration Board PN MAATGM0001-SMB (available upon request).

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